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T42 – Transputer Design in FPGA (Year Three Design Status Report)

Fringe Presentation

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Abstract. Our IMS-T425 compatible Transputer design in FPGA has so far taken over 300 design days. Up to last year, minimal effort was spent for verification. Now a regression test bench has been brought in place, which is targeted to verify the design conformance after any changes. This T42 Transputer Verification Suite is based on a TVS-1 work from Michael Bruestle, and compares the register output of 54 selected instructions versus a true T425 *golden reference* for up to thousands of data samples. It has already helped in T42 micro-code debugging and hardware refinement.

Keywords. T42, Transputer, FPGA, scheduler, links, micro-code, regression test, TVS-1

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